FAST DATA ACCESS MODE IN A MEMORY DEVICE

TECHNICAL FIELD OF THE INVENTION

[0001]   The present invention relates generally to memory devices and in particular the present invention relates to fast data access in memory devices.

BACKGROUND OF THE INVENTION

[0002]   Memory devices are typically provided as internal, semiconductor, integrated circuits in computers or other electronic devices. There are many different types of memory including random-access memory (RAM), read only memory (ROM), dynamic random access memory (DRAM), and synchronous dynamic random access memory (SDRAM).

[0003]   As microprocessor speeds continue to increase, memories have to keep pace. Synchronous memories have done so with high clock speeds as well as pipelined data architectures. Pipelined architectures are typically used to divide the data path into multiple, shorter segments in order to achieve higher clock speeds. However, the higher the clock frequency, the faster the required data access time.

[0004]   Pipelined architecture also increases the read latency. For example, a three stage data pipeline can accommodate read latencies of up to three clock cycles. The final stage determining the data access time for the read latency of three clock cycles.

[0005]   For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for a way to decrease data access time in a memory device having a pipeline architecture.

SUMMARY

[0006]   The above-mentioned problems with data access times in a memory device and other problems are addressed by the present invention and will be understood by reading and studying the following specification.

[0007]   The present invention encompasses a fast data access circuit that increases the rate at which data is output from the memory device as an input clock frequency increases. The circuit comprises a clock delay circuit that applies a user selectable time delay to the input clock signal. In one embodiment, the delay decreases as the clock frequency increases. The clock delay circuit generates a delayed clock signal;

[0008]   A control circuit generates a mode control signal. In one embodiment, this circuit is a mode/configuration register that is loaded with a configuration word to set the modes/configurations of the memory device.

[0009]   A multiplexing circuit has one input coupled to the input clock signal and a second input coupled to the delayed clock signal. The multiplexing circuit selects between the two inputs based on the mode control signal.

[0010]   A data output register is coupled to a memory array of the memory device. The rate at which the data bits are output is controlled by the selected clock output by the multiplexer circuit.

[0011]   Further embodiments of the invention include methods and apparatus of varying scope.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012]   Figure 1 shows a block diagram of one embodiment of a fast data access circuit of the present invention.

[0013]   Figure 2 shows a table of one embodiment of the mode register of the present invention.

[0014]   Figure 3 shows a block diagram of one embodiment of the clock delay circuit of the present invention.

[0015]   Figure 4 shows a more detailed logic diagram of one embodiment of the data buffer and output buffer in accordance with Figure 1.

[0016] Figure 5 shows a more detailed logic diagram of one embodiment of the clock multiplexer and FIFO control logic in accordance with Figure 1.

[0017] Figure 6 shows a timing diagram of one embodiment of a standard operating mode for read timing of a memory device of the present invention.

[0018] Figure 7 shows a timing diagram of one embodiment of a fast data access mode for read timing of a memory device of the present invention.

[0019] Figure 8 shows a block diagram of an electronic system in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION

[0020] In the following detailed description of the invention, reference is made to the accompanying drawings that form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims and equivalents thereof.

[0021] Figure 1 illustrates a block diagram of one embodiment for a fast data access circuit of the present invention. This circuit is implemented in a three-stage data pipelined architecture. In one embodiment, the first stage is from a sense amplifier 130 to a data latch 123. The second stage is from the data latch 123 to a data FIFO 109. The third stage is from the data FIFO 109 to the DQ pad of the memory device. The present invention, however, is not limited to any quantity of pipelined stages nor to any certain composition of each stage.

[0022] An address and clock signal are input to an address buffer/burst counter 117. The address buffer/burst counter 117 provides the addresses to the memory bank 113 for further decoding by the column decoding circuitry 119. As is well known in the art, the burst counter 117 sequentially counts through a predetermined number of addresses and provides these addresses to the memory bank 113 so that the predetermined number of data bits can be output.

[0023] For purposes of clarity, only one cell array 115 and two column decode circuits 119 are shown. However, a memory bank may be comprised of millions of cell arrays 115, each column of cell arrays having a separate column decode circuit 119. The memory bank further includes a data amplifier 121 that combines the differential data from the cell array and outputs the data to a latch 123. The latched data is output from the memory bank 113 through a data output buffer 125. The operation of the circuitry of the memory bank 113 is well known in the art and is not discussed further.

[0024] The input address signals are also input to a mode/configuration register 101. As discussed subsequently with reference to Figure 2, the mode/configuration register 101 accepts a configuration word, from the address lines, to set up the various modes of the memory device. Two such modes are the standard mode and the fast data access mode.

[0025] The configuration word to the mode/configuration register 101 also selects the clock speed of the input clock signal (CLK) to the circuit. In one embodiment, there are four selectable clock speeds: 143 MHZ, 166 MHz, 200 MHz, and 250 MHz. However, the quantity of clock speeds is determined by the quantity of bits available in the configuration word for this function. If only one bit is available, only two clock speeds are selectable. If more than two bits are available, more than four clock speeds are selectable.

[0026] In an alternate embodiment, the mode is selected by a state machine or other control circuit of the memory device. Such a control circuit may select the desired clock speed using control signal outputs.

[0027] The clock signal is input to a clock delay circuit 103. This circuit 103 provides the clock with a set delay that depends on the selected clock speed in the

mode/configuration register 101. The clock delay circuit 103 is discussed subsequently in greater detail with reference to Figure 3.

[0028] In one embodiment, there are four selectable input clock speeds for the fast data access mode that are selected by an output signal from the mode/configuration register 101 to the clock delay circuit 103. The present invention is not limited to any predetermined quantity of delays. Alternate embodiments may have more or less than four selectable delays, including a continuously variable delay.

[0029] The delayed clock, CLK_FDA, is output from the clock delay circuit 103 and input to a clock multiplexer circuit 105. The standard clock, CLK_STD, is also input to the clock multiplexer circuit 105. A standard mode select output (STD_MODE) from the mode/configuration register 101 is used as a selection signal for the multiplexer 105. In one embodiment, when STD_MODE is a logical high signal, the standard clock is selected. When STD_MODE is a logical low signal, the fast data access clock (CLK_FDA) is selected to be output from the multiplexer 105. Alternate embodiments use inverse logic states for the STD_MODE signal to select between the standard clock and the fast data access mode clock.

[0030] The clock selected by the multiplexer 105 is output to first-in-first-out (FIFO) control logic 107. The FIFO control logic 107 is responsible for generating the data output control pulses to the data FIFO circuit 109. These signals are illustrated as MXD<1:0> and MXQ<1:0> and are used to enable different portions of the data FIFO circuit 109 to permit the input data (DR) from the memory bank 113 to travel through the third stage at different speeds, depending on the selected mode. The input data (DR) may be part of a data stream if a burst mode has been selected in the mode/configuration register 101.

[0031] Alternate embodiments use other circuits to output the data instead of the data FIFO circuit 109. For example, some type of data output register that can temporarily store data for subsequent output controlled by either the standard clock or the fast data access clock is encompassed by the present invention.

[0032] A data output buffer 111 outputs the DRQ data from the data FIFO circuit 109 as DQ. In one embodiment, DQ is coupled to the output pin of the memory device. The third

stage circuitry is illustrated in greater detail and discussed subsequently with reference to Figure 4.

[0033]   Figure 2 illustrates a table of one embodiment of a memory mode/configuration register of the present invention. The bits (M11 – M0) of the configuration word program the various modes of the memory device. These bits set the clock frequency (CLK FREQ), burst mode (WB), operation mode (OP MODE), column access strobe latency (CAS LATENCY), burst type (BT), and burst length. Alternate embodiments set other memory device configurations and/or use different bits and quantity of bits to perform these functions.

[0034]   The memory mode (i.e., standard or fast data access) is selected by bits M8 and M7 of the configuration word, as illustrated in the mode selection area 201 of the table of Figure 2. One of the four available clock frequencies 200 is selected by the M11 and M10 bits of the configuration word. If the standard mode has been selected, the M11 and M10 bits are not relevant since the clock speed is less than 143 MHz in this embodiment.

[0035]   The table of Figure 2 is for illustration purposes only and does not limit the invention to any one memory mode or configuration table. Alternate embodiments may use configuration words having different lengths than is illustrated or different bit states to program a particular memory configuration.

[0036]   Figure 3 illustrates a logic diagram of one embodiment of the clock delay circuit 103 of Figure 1. This embodiment includes four selectable delays that are selected by the M11 and M10 bits of the configuration word of the mode/configuration register. Alternate embodiments may use different quantities of delays, different delay lengths, and different types of delay elements.

[0037]   The clock delay circuit 103 is comprised of four delay circuits (DELAY_0 – 3) that are each made up of four inverters 320 – 323 that cause the delay in the input clock (CLK_STD). Each delay is selected by selection logic 301 – 304 that, in one embodiment, comprise a NAND gate 311 and an inverter 309. This logic 309 and 311 activates a transmission gate 313 when the input signals (M11 and M10) are true.

[0038]   When the shortest delay is activated, DELAY_3 is the only delay used. In this case, the CLK_STD signal is input through the first activated transmission gate 313 after experiencing four gate delays. The delayed signal is output as the CLK_FDA.

[0039]   When a somewhat longer delay is necessary, both DELAY_3 and DELAY_2 are selected. In this case, the first transmission gate 313 is disabled and the second transmission gate 314 is enabled. The input clock signal, CLK_STD, is then input through eight gate delays before being output through the second transmission gate 314 as CLK_FDA.

[0040]   Selecting the third longest delay causes DELAY_1 – DELAY_3 to be selected. In this case, the first two transmission gates 313 and 314 are disabled and the third transmission gate 315 is enabled. The input clock is then input through twelve gate delays before being output through the third transmission gate 315 as CLK_FDA.

[0041]   Finally, selecting the fourth delay causes DELAY_0 – DELAY_3 to be selected. In this case, only the last transmission gate 316 is enabled so that the input clock signal goes through sixteen inverter gate delays before being output through the last transmission gate 316 as CLK_FDA.

[0042]   The clock delay circuit 103 also includes additional inverters 330 – 333 that are used to provide the proper states of the input signals for decoding 330 and 331 as well as adding additional delay 323 and 333 at the output of the circuit 103. The logic illustrated in Figure 3 is for purposes of illustration only. The present invention is not limited to any one circuit architecture to generate the separate delays used in the fast access mode.

[0043]   As discussed above in Figure 2, M11 and M10 set the input clock frequency for the memory device. Since these signals also set the delay for each frequency, it can be seen from the clock delay circuit 103 that the higher the clock frequency indicated by M11 and M10, the shorter the delay required to generate CLK_FDA.

[0044]   Figure 4 illustrates a logic diagram of the data FIFO 109 and data out buffer 111 as discussed in Figure 1. The data FIFO uses the MXD<1:0> and MXQ<1:0> pulses from the FIFO control logic as control inputs; MXD<1:0> controls the latching of the data and

MXQ<1:0> controls the output of the data. DR is the data bit that is output from the memory cell to be latched into the FIFO 109.

[0045]   The access of DR to one latch 403 is controlled by the transmission gate coupled to MXD<0>. In one embodiment, when this signal is a logic high, the DR bit is latched into the top latch 403. An inverter 407 inverts the MXD<0> signal for application to the inverted control connection of the transmission gate 401.

[0046]   The DR bit is latched into the bottom latch 413, through the bottom transmission gate 411, when MXD<1> is a logic high. An inverter 409 inverts MXD<1> for application to the inverted control connection of the transmission gate 411.

[0047]   The outputs of each of the latches 403 and 413 are output through an inverter 405 and 415 to a respective transmission gate 419 and 423. The output of the data bit that was latched in the top latch 403 is controlled through one transmission gate 419. The control signal MXQ<0> is input to one control input of the transmission gate 419 and through an inverter 417 for application to the inverted control input of the transmission gate 419.

[0048]   The second transmission gate 423 controls the output of the bit latched into the bottom latch 413. The control signal MXQ<1> is input to one control input while an inverter 421 inverts the control signal into the inverted control input of the transmission gate 423.

[0049]   The bit output through the output transmission gates 419 or 423 is latched into an output latch 425 before going through an inverter 427 and output as DRQ. DRQ is then input to the data out buffer 111 to be output as the DQ signal.

[0050]   The operation of the data FIFO 109 is best illustrated with reference to the timing diagrams of Figures 6 and 7. The timing diagram illustrated in Figure 6 shows the standard operating mode for read timing with a column address strobe latency of three. The timing diagram illustrated in Figure 7 shows the fast data access mode of the present invention for read timing with a column address strobe latency of three.

[0051] While one latch of the FIFO is being loaded from the DR input, the other latch is driving its data out onto the DRQ bus. This is accomplished with the MXD and MXQ signals.

[0052] By comparing the MXQ<1:0> signal of Figure 7 with the same signal of Figure 6, it can be seen that the fast data access mode MXQ<1:0> occurs sooner than its Figure 6 counterpart. Since the MXQ<1:0> signals control the output of the data through the data FIFO, the data is output from the FIFO at a faster rate than under the standard operating mode. Figure 7 also shows that this results in t_{AC} being shorter than its counterpart time in Figure 6, thus indicating the faster data access. The rate at which data is loaded into the FIFO is unchanged.

[0053] Figure 5 illustrates a more detailed logic diagram of one embodiment of the clock multiplexer 105 and FIFO control logic 107 of Figure 1. This diagram is for purposes of illustration only. In alternate embodiments, the multiplexer 105 and control logic 107 may be implemented in other ways.

[0054] The logic diagram comprises a set of transmission gates and an inverter that make up the multiplexer 105. When the mode control signal (STD_MODE) is high, CLK_STD is allowed through the lower transmission gate 501 while the upper transmission gate 502 is turned off. When the mode control signal is low, CLK_FDA is allowed through the upper transmission gate 502 while the lower transmission gate 501 is turned off.

[0055] The FIFO control logic section 107 is comprised of a toggle flip flop 505 that generates the MXQ<1:0> signals and a toggle flip flop 506 with a delay element 511 that generates the MXD<1:0> signals. The control logic section 107 includes two enable input signals, MXQ_EN and MXD_EN, that originate from another logic block (not shown). These signals and their relationship with the outputs of the FIFO control logic 107 are illustrated in the timing diagrams of Figures 6 and 7.

[0056] In the standard operating mode, the enable signals are both switched at the same time and CLK_STD is used to generate both MXD and MXQ signals. The MXQ circuit 505 is enabled by the MXQ_EN signal being at a logic high. The MXD circuit 506 is enabled by the MXD_EN signal being at a logic high.

[0057] In the fast data access mode, MXQ_EN is switched on first and used with the CLK_FDA signal to generate the MXQ signals. The MXD signals are generated from CLK_STD with MXD_EN.

[0058] The output control signals from the MXD toggle flip flop 506, during the standard operating mode (with a CAS latency of 3), are illustrated in the MXD<1:0> lines of the timing diagram of Figure 6. The output control signals from the MXQ toggle flip flop 505, during the standard operating mode (with a CAS latency of 3), are illustrated in the MXQ<1:0> lines of the timing diagram of Figure 6. The same lines of Figure 7 illustrate the respective outputs of these circuits 505 and 506 during the fast data access mode.

[0059] Figure 8 illustrates a functional block diagram of a memory device 800 of one embodiment of the present invention that is coupled to a controller circuit 810. The controller circuit 810 may be a microprocessor, a processor, or some other type of controlling circuitry. The memory device 800 and the controller 810 form part of an electronic system 820. The memory device 800 has been simplified to focus on features of the memory that are helpful in understanding the present invention.

[0060] The memory device includes an array of memory cells 830. The memory cells are non-volatile floating-gate memory cells and the memory array 830 is arranged in banks of rows and columns.

[0061] An address buffer circuit 840 is provided to latch address signals provided on address input connections A0-Ax 842. Address signals are received and decoded by a row decoder 844 and a column decoder 846 to access the memory array 830. It will be appreciated by those skilled in the art, with the benefit of the present description, that the number of address input connections depends on the density and architecture of the memory array 830. That is, the number of addresses increases with both increased memory cell counts and increased bank and block counts.

[0062] The memory device 800 reads data in the memory array 830 by sensing voltage or current changes in the memory array columns using sense/latch circuitry 850. The sense/latch circuitry, in one embodiment, is coupled to read and latch a row of data from

the memory array 830. Data input and output buffer circuitry 860 is included for bi-directional data communication over a plurality of data connections 862 with the controller 810). Write circuitry 855 is provided to write data to the memory array.

[0063] Control circuitry 870 decodes signals provided on control connections 872 from the processor 810. These signals are used to control the operations on the memory array 830, including data read, data write, and erase operations. In one embodiment, the control circuitry 870 executes the methods of the present invention.

[0064] The fast data access circuit 100 of the present invention may be implemented in the electronic system as illustrated in Figure 8. Portions of the control registers 880, memory array 830, and column decoder 846 are also illustrated in Figure 1 as being part of the circuit 100. These circuit elements are not required to be part of the fast data access circuit 100.

[0065] The flash memory device illustrated in Figure 8 has been simplified to facilitate a basic understanding of the features of the memory. A more detailed understanding of internal circuitry and functions of flash memories are known to those skilled in the art.

[0066] The previous discussion of the present invention refers to synchronous flash memory as being a memory device that can incorporate the fast data access circuit of the present invention. However, the present invention is not limited to any one type of memory. Nor is the present invention limited to any one type of flash memory. For example, the present invention can be incorporated into NAND-type flash device, a NOR-type flash device, or any other type of memory device that would benefit from increasing the throughput of data through a data pipeline architecture.

CONCLUSION

[0067] In summary, the circuit of the present invention provides fast data access at higher clock frequencies through the use of additional mode/configuration register settings. These settings are used to set the clock frequency and to switch the memory device from its standard operating mode to a fast data access mode. In this mode, a delayed clock is generated and used to clock data out of the final stage of the pipelined architecture.

[0068] Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement that is calculated to achieve the same purpose may be substituted for the specific embodiments shown. Many adaptations of the invention will be apparent to those of ordinary skill in the art. Accordingly, this application is intended to cover any adaptations or variations of the invention. It is manifestly intended that this invention be limited only by the following claims and equivalents thereof.